REMARKS

I. Claim Objections

Claim 20 was objected to as being dependent from cancelled claim 19; hence, claim 20 has been amended to be dependent from claim 18. Claim 32 was objected to because of the repetition of "the"; hence, claim 32 has been amended to delete one "the".

II. Claim Rejection – 35 USC § 102

Claims 1-4, 6-11, 13-18, 20-22 and 28-32 were rejected under 35 USC § 102 as being anticipated by Ovens. Recitations of dependent claims 6, 13, 20, 29 have been incorporated into independent claims 1, 10, 16, and 28, respectively, and these dependent claims 6, 13, 20, 29 have been canceled.

A. Examiner's Misunderstandings with respect to the downstream Latch

The Examiner's technical analysis of the Ovens reference is incorrect in many aspects. Using independent claim 1 as an example, the Examiner stated that:

> "a downstream latch (transmission gate between lines N4 and N7), having an open state and a close state (as is inherent to transmission gates), a pair of inputs coupled to the first level shifter and the delay element and an output coupled to the second circuit (as shown in fig. 1), to generate an output data signal (Y128) in response to the level shifted data signal and the delayed clock signal, with the triggering clock edge of the delayed clock signal switching the downstream latch from the close state to the open state (via CLKT and CLKF) (column 3, line 51 thru column 4, line 19)"

The errors in this analysis are as follows:

(1) Applicants' claim language clearly defines the downstream latch as being coupled to the output of the first level shifter. Without that downstream relationship of the downstream latch to the first level shifter, the invention could in no way perform the function of avoiding the mismatch that can be generated in the level shifted data signal at the output of the first level shifter. Applicants have underlined above some of the claim language that places the downstream latch at the output of the first level shifter. To the contrary, in Ovens the transmission gate between lines N4 and N7 cited by the Examiner for the downstream latch is upstream of the data level shifter 128 (its output goes eventually goes to the data level shifter 128).

(2) The transmission gate between lines N4 and N7 is part of the latch 118 (flip-flop), which the Examiner has cited against the flip-flop recited in Applicants' claim 1; hence, cannot be a separate element, the downstream latch.

(3) The Examiner is incorrect in stating that a latch "is inherent to transmission gates". To the contrary, a transmission gate passes a signal or does not pass a signal based upon the clock signals, and a transmission gate does not latch (hold) a signal (e.g., during part of a clock cycle), as a latch does.

B. Examiner's Misunderstanding with respect to the delayed clock signal

Again, with respect to claim 1, the Examiner stated that:

> "a delay element (not shown in 108) coupled to the clock source and responsive to the clock signal to generate a delayed clock signal having a triggering clock edge (column 3, lines 43-61)"

In claim 1 recites "a flip-flop...to generate a second data signal...in response the clock signal and the "downstream latch ... to generate an output data signal in response to the ....delayed clock signal....". The delay in the clock signal is introduced between the clock signal used by the flip-flop and the delayed clock signal used by the downstream latch.

To the contrary, in Ovens, the latch 118 uses the clock signals CLKT and CLKF and the transmission gate between N4 and N7 also uses the same clock signals CLKT and CLKF – there is no delayed clock between the two elements. In other words, to the extent that the CTS buffer of Ovens introduces a delay, it applies both to the clock signals used for both the flip-flop and the transmission gate, since both elements use the same clock signals. In Ovens the CTS buffer (column 3, lines 53-58) has "the purpose of the buffer is to equalize all of the clock delays". The CTS buffer is placed between the clock signal 106 of the I/O section 102 and the clock signal of the core 104; hence, it delays all the clock signals equally.

Although Ovens teaches a voltage level data shifter which is downstream of the flip-flop (FIG. 1) or upstream of the flip-flop (FIG. 2), Ovens does not teach:

(1) a flip-flop and a downstream latch with the voltage level shifter interposed between the flip-flop and the downstream latch; and

(2) the flip-flop using a clock signal and the downstream latch using a delayed clock signal, with a delay element delaying the clock signal to provide the delayed clock signal and a triggering clock edge of the delayed clock signal being used to trigger the downstream latch.

In independent claim 28 the term "downstream slave latch" is used instead of "downstream latch".

C. Amendments to Independent claims to incorporate Dependent Claims

As already mentioned, an additional amendment has been made to the independent claims 1, 10, 16 and 28 in the hopes of clarifying the invention to the Examiner, with this limitation previously being found in the dependent claims 6, 13, 20, and 29, thus no new matters are introduced, and no new searches are required. Independent claims 1, 10, 16 and 28 now recite (similar language has been added to claim 28):

> "wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the downstream latch"

This additional recitation clarifies that the delayed clock signal must be delayed to the extent that the rising and falling edges of the level shifted data signal have already arrived. In other words, it quantifies the minimum delay needed, There is no teaching or suggestion of this solution in Ovens.

D. Independent Claims 10, 16, and 28 and dependent claims

The above arguments made with respect to independent claim 1 are equally applicable to independent claims 10, 16 and 28. The dependent claims should be allowable because of at least the reasons described with respect to the independent claims.

E. Further Discussion of Applicant's invention, as claimed in the independent claims

Applicant's invention, as recited in the independent claims, addresses the fact that voltage level shifters introduce extra timing skew between the rising and falling edges (signal transitions) of the data signals and clock signals, as shown by the cross hash

lines in the "level shifted data" of FIG. 4 of Applicant's drawings. In other words, the data shifted signal has a time period during which the rising and falling data edges are mismatched. The triggering edge of the delayed clock signal for triggering the downstream latch is delayed by the delay element until after an arrival of the rising and falling data edges (signal transistions) at the of the downstream latch.

Paragraphs 18-20 (paragraph 21 is a summary) of Applicant's specification describes how the introduction of the downstream latch ("downstream slave latch" in independent claim 28) allows for the timing of the signal transistions of the output data signal of the downstream latch to be tied only to one clock edge instead of two edges, the "triggering clock edge" for the downstream latch. There are no such teaches in the Ovens reference.

Applicants incorporate by reference the presentation provided in the response to the First Office Action which includes a "Description of Ovens and problem addressed" and "Applicant's Claimed invention addresses a different problem than Ovens", which is equally relevant to the Examiners new interpretation of Ovens.

III. Reasons for Entering this Amendment After Final

Applicants believe this amendment should be entered and all claims allowed. To do otherwise means that the issues on Appeal will center on the Examiner's multiple technical misunderstandings both as to the Ovens reference and Applicants' claimed invention. Moreover, the Examiner introduced this new interpretation of Ovens for the first time in his Final Office Action and then characterized this new interpretation as a "new ground(s) of rejection". Failure to enter this amendment would be particularly inappropriate in view of Applicants having previously made a detailed and complete explanation of the claimed invention and the Ovens reference in Applicants' earlier response to the First Office Action, in which Applicants explained away earlier and different technical misunderstandings by the Examiner.

In any case, entry of amendments correcting Examiner's objections to the claims and incorporating the dependent claims into the independent claims places this case in a better condition for Appeal.

IV. Conclusion

Claims 1-4, 7-11, 12-18, and 21-22, and 28, and 30-32 were pending prior to this response. In this response, claims 6, 13, 20 and 29 have been canceled. Previously, in the response to the first Office Action, claims 5, 12, 19, and 23-27 were canceled. In view of the foregoing amendments and arguments, Applicant submits that the pending claims are in condition of allowance. Early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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